# A Digital Approach for Testing Analog Memories

D. Ronga, P. Girard, A. Virazel
LIRMM – University of Montpellier / CNRS
Montpellier, France
dronga, girard, virazel@lirmm.fr

***Abstract*—Most of the modern electronic devices require memory components to operate. Testing memory components is crucial to ensure the reliability of the electronic devices that depends on it. As the technology shrink, the integration density of transistors increases, making nanometer-scaled transistor-based memories, such as Static Random-Access Memory (SRAM), more sensitive to manufacturing defects and manufacturing non-idealities. The increased sensitivity of these components makes their fault mechanisms more complex, requiring tests capable of satisfying complex fault sensitization and detection conditions. As test complexity grows, shifting to digital test tools capable of managing the complexity (e.g., Fault Simulator, Automatic Test Pattern Generator) constitute a promising approach. This talk compiles published work on shifting SRAM test to the digital domain. The digital representation for test of a SRAM is introduced, and the digital representation of complex fault mechanisms is presented. The coverage of complex dynamic memory Functional and Structural Fault Models (FFM and SFM) is discussed in the digital domain, and obtained results are presented.**